CLAIMS

1. A method for forming electrically conductive bumps on a wafer comprising the steps of:

providing a wafer having an active surface, a plurality of conductive elements formed on the active surface, and a passivation layer insulating said plurality of conductive elements from each other,

sputter depositing a first metal layer on top of said plurality of conductive elements and said passivation layer,

printing a plurality of bumps of an insulating material each on top of one of said plurality of conductive elements,

heat treating said plurality of bumps at a temperature of at least 100°C,

sputter depositing a second metal layer on top of said plurality of bumps and said first metal layer, and

patterning and removing said first and said second metal layer in areas in-between said plurality of bumps.

2. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of forming said plurality of conductive elements spaced-apart by at least 100 μm.

3. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of forming said plurality of conductive elements in aluminum or copper.

4. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of forming said passivation layer in an insulating material.

5. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of sputter depositing said first metal layer in a material selected from the group consisting of Al, Ni, Ti, W, Cu, Cr and alloys thereof.

6. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of sputter depositing said first metal layer to a thickness not higher than 50 μm.

7. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique.

8. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in a polymeric material.

9. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in polyimide.

10. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique to a width of at least 50 μm.

11. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique to a thickness of at least 20 μm.

12. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in a polymeric-based paste.

13. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in a solvent-containing polymeric paste.

14. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of depositing said second metal layer in a material selected from the group consisting of Al, Ni, Ti, W, Pt, Pd, Cu, Cr, Ag, Au, In, Sn, Pb and alloys thereof.

15. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of patterning said first and said second metal layer by a photolithographic method.

16. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of removing said first and said second metal layers by a photolithographic and a wet etch method.

17. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface comprising:

a semiconductor wafer having an active surface on top,

a plurality of conductive elements formed on said active surface spaced-apart by at least 50 μm,

a passivation layer insulating said plurality of conductive elements from each other,

a plurality of electrically conductive pads each on one of said plurality of conductive elements,

a plurality of electrically insulative bump each on one of said plurality of a first electrically conductive pads, and

a plurality of a second electrically conductive pads each on top of one of said plurality of electrically insulative bumps in electrical communication with a corresponding one of said plurality of a first electrically conductive pads and one of said plurality of conductive elements.

18. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of a first electrically conductive pad and said plurality of a second electrically conductive pad are formed of the same electrically conductive metal.

19. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of a first electrically conductive pad and said plurality of a second electrically conductive pad are formed of a material selected from the group consisting of Al, Ni, Ti, W, Pt, Pd, Cu, Cr, Ag, Au, In, Sn, Pb or alloys thereof.

20. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of electrically insulative bumps is formed of a polymeric material.

21. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of electrically insulative bumps is formed of polyimide.

22. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of electrically insulative bumps is formed of a solvent-containing polymeric paste.

23. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of electrically insulative bumps is formed to a width between about 50 μm and about 100 μm.

24. A semiconductor wafer having a plurality of electrically conductive bumps formed on an active surface according to claim 17, wherein said plurality of electrically insulative bumps is formed to a thickness of at least 20 μm.